In the Specification:

Kindly amend paragraph 29, beginning on page 11, as set forth below:

[0029]   Thus, the sparse ADC 140 determines a difference between the output voltage V_{out} and the desired system voltage V_{system} and provides the error signal S_E therefrom. The duty cycle processor 150 then employs the error signal S_E to provide a digital duty cycle signal S_D (*e.g.*, a four or an eight bit digital signal representing a duty cycle) to control a duty cycle of at least one switch of the power converter. An embodiment of a sparse ADC 140 and duty cycle processor 150 are disclosed in U.S. Patent Publication No. 2005/0169024 ~~Application Serial No. [Attorney Docket No. ENP-001]~~, entitled "Controller for a Power Converter and a Method of Controlling a Switch Thereof," to Dwarakanath, et al., which is incorporated herein by reference.

Kindly amend paragraph 33, beginning on page 13, as set forth below:

[0039]   Thus, the modulator 180 supplies a signal that is typically constructed to form a pulse width modulated signal S_{PWM} to control the duty cycle for at least one switch of the power converter. The modulator 180 can also supply a complement of the signal to control the duty cycle for at least one switch of the power converter (*e.g.*, a complementary pulse width modulated signal S_{1-PWM}). The pulse width modulated signal S_{PWM} and the complementary pulse width modulated signal S_{1-PWM} are then fed to the driver 190. Additionally, an embodiment of a modulator is disclosed in U.S. Patent Publication No. 2005/0168205 ~~Application Serial No. [Attorney Docket No. ENP-002]~~, entitled "Controller for a Power Converter and Method of Controlling a Switch Thereof," to Dwarakanath, et al., which is incorporated herein by reference.